Utpal Bora

Research Associate in the dept. of Computer Science & Technology at UNIVERSITY OF CAMBRIDGE

Education

Aug 2014 – May 2022 Integrated M.Tech. & Ph.D. in Programming Languages and Compilers in the Dept. of Computer Science & Engineering at IIT Hyderabad (IITH), under the supervision of Dr. Ramakrishna Upadrasta and Dr. Saurabh Joshi.

Aug 2005 – Jul 2009 **B.Tech.**, Electronics & Communication Engineering, Dr. B. R. Ambedkar National Institute of Technology Jalandhar (NIT Jalandhar).

Publications

Journal Articles

- Jain, S., **Bora**, **U.**, Kumar, P., Sinha, V. B., Purini, S., & Upadrasta, R. (2019). An Analysis of Executable Size Reduction by LLVM Passes. *CSI Transactions on ICT*, 7(2), 105–110. & https://doi.org/10.1007/s40012-019-00248-5

Conference Proceedings

Bora, U., Vaishay, S., Joshi, S., & Upadrasta, R. (2021). OpenMP aware MHP Analysis for Improved Static Data-Race Detection. In 2021 IEEE/ACM 7th Workshop on the LLVM Compiler Infrastructure in HPC (LLVM-HPC) (pp. 1–11). To be published. 6 https://doi.org/{10.1109/LLVMHPC54804.2021.00006}

Miscellaneous

- **Bora**, U., Das, S., Kukreja, P., Joshi, S., Upadrasta, R., & Rajopadhye, S. (2021). LLOV: A Fast Static Data-Race Checker for OpenMP Programs [Technical Talk, HiPEAC].
- **Bora**, **U.**, Das, S., Kukreja, P., Joshi, S., Upadrasta, R., & Rajopadhye, S. (2020). LLOV: A Fast Static Data-Race Checker for OpenMP Programs [Technical Talk, LLVM Performance Workshop at CGO].
- Kukreja, P., Shukla, H., & **Bora**, **U.** (2019). DataRaceBench FORTRAN [Open Source Benchmark, Github].
- Dangeti, T. K., **Bora**, **U.**, Das, S., Grosser, T., & Upadrasta, R. (2017). Improved Loop Distribution in LLVM using Polyhedral Dependences [Lightning Talk, LLVM-HPC Workshop at SC].
- **Bora**, **U.**, Doerfert, J., Grosser, T., & Upadrasta, R. (2016). GSoC 2016: PolyhedralInfo Polly as an Analysis Pass in LLVM [Lightning Talk, US LLVM Dev Meet].
- **Bora**, **U.**, & Pratik, B. (2016). Introduction to LLVM Compiler Infrastructure [Invited Talk, GDG DevFest Hyderabad].
- Das, S., Kumar, D. T., **Bora**, **U.**, & Upadrasta, R. (2016). A Comparative Study of Vectorization in Compilers [Student Research Symposium, HiPC].

Projects

Loop Nest Optimization: Developed an infrastructure in LLVM to perform loop nest optimizations (LNO) such as loop distribution, statement reordering, and loop vectorization using polyhedral reduced dependence graph. This work was presented in LLVM-HPC [7] at SC'17.

Projects (continued)

DRB FORTRAN: Implemented a benchmark of OpenMP kernels in FORTRAN for data race detection. It contains kernels with data races and kernels without known races. The benchmark is released under open source licence (Github).

LLOV: Developed LLOV- A Fast Static Data-Race Checker for OpenMP Programs [1]. The tool is available to download for free (Github).

Experience

Feb 2022 – Present PostDoc in the Computer Laboratory at University of Cambridge. Exploring new static analyses and program transformations to extract fine-grained parallelism.

Aug 2015 – Jan 2016 Research Internship at AMD India Pvt. Ltd. in the Compilers team. Worked on using Polyhedral program analysis in LLVM.

Dec 2009 – May 2014 Software Developer at DXC Technology (formerly CSC India Pvt. Ltd.): Worked on design and development of business applications for the insurance domain. Experience in C# for frontend and Microsoft SQL Server for backend development.

Recognition

Awards and Achievements

July 2022 Summer School organized by HiPEAC Network in Fiuggi, Italy.

Feb 2020 Awarded a *student travel grant* by the ACM SIGPLAN to attend CGO 2020.

Aug 2018 Selected for the ECOOP/ISSTA '18 SUMMER SCHOOL (with travel grant), Amsterdam, Netherlands. (Could not attend)

Awarded *student travel grants* by the LLVM Foundation to attend the LLVM Developers' Meetings in 2016 & 2017.

June 2016 Successfully completed **Google Summer of Code** project *Polly as an Analysis Pass in LLVM* with the LLVM Compiler Infrastructure organization. GSoC Project, Blog.

Aug 2015 Awarded the **Visvesvaraya Ph.D. Fellowship**, (MeitY, India).

Jun 2015 Represented IIT Hyderabad in a research collaboration visit to Ritsumeikan University, Japan.

Mar 2015 Received the **Academic Excellence Certificate** for outstanding academic performance in the M.Tech. program at IIT Hyderabad.

May 2014 Secured All India Rank 239 among 155k applicants (**99.8% percentile**) in GATE-2014 examination in CS & IT branch having done B.Tech in ECE branch.

Oct 2010 Awarded **Star Performer of the Quarter** at CSC India Pvt. Ltd. for outstanding performance in Q3.

Committee and Volunteer-ship

Committee TPDS Reviewer, ECOOP'23 AEC, CGO'23 AEC, ASPLOS'23 AEC, MICRO'22 AEC, ISSTA'22 AEC, PLDI'22 AEC, CGO'22 AEC, ASPLOS'22 AEC, MICRO'21 AEC, ASPLOS'21 AEC, PACT'21 AEC, ISSTA'21 AEC, ECOOP'21 AEC, SC'21 AD/AE, JSys AEB, IndoSys'19 Subreviewer

Volunteer Student volunteer at SPLASH'21, PLDI'21, POPL'21, ICSE'21, ACCU'21, IndoSys'18

Summer School Helped to organize the Sutton Trust Summer Schools 2022 at University of Cambridge.

Workshop Helped to organize a workshop on Program Analysis and Compilers at CDAC Hyderabad in February 2020.

Teaching Experience

Supervised Tripos Part II courses *Principles of Communications* and *Optimising Compilers* at the University of Cambridge.

Teaching assistant for Introduction to Programming, Data Structure and Programming, Principles of Programming Languages, Compiler Design, Compiler Engineering (LLVM), Compiler Optimizations, and Topics in Compiler Optimizations courses at IIT Hyderabad.

2016-2020 Co-taught in *Compiler Engineering* courses at IIT Hyderabad using the LLVM Infrastructure.

Skills

Coding C, C++, OpenMP, LLVM, Python, sql, xml/xsl, LTFX, ASP.NET, C#.NET.

Databases Mysql, Microsoft sql Server.

Web Dev HTML, css, JavaScript, Apache Web Server, IIS Web Server.